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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/823,060 | 04/13/2004 | Wei Fu | AMCC10180 | 3987 |

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| EXAMINER | |
|---|---|
| NGUYEN, MINH T | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2816 | |

DATE MAILED: 06/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/823,060 | FU ET AL. | |
| | Examiner | Art Unit | |
| | Minh Nguyen | 2816 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6,7,11 and 16* is/are rejected.

7)☒ Claim(s) *3-5,8-10,12-15 and 17-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 April 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1)☒ Notice of References Cited (PTO-892)
2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5)☐ Notice of Informal Patent Application (PTO-152)
6)☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to because the recited connections in claims 12 and 17 do not consistent with the connections shown in figure 4. Specifically, (i) the third latch 430 in figure 4 does not receive a second delayed version of the clock signal as recited (rather it receives an inverse of the second delayed version of the clock signal), (ii) the fourth latch 432 does not receive the second delayed version of the data signal and the inverse of second delayed version of the clock signal (rather it receives an undefined data signal Q2 and the second delayed version of the clock signal). Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner,

the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Objections*

2. Claims 3, 8 and 18 are objected to because of the following informalities:

In claim 3, line 6, "the incoming signal" should be changed to -- the incoming data signal -- for consistency, see line 2 of claim 1.

In claim 8, line 8, "the incoming signal" should be changed to -- the incoming data signal -- for consistency, see line 2 of claim 6.

In claim 18, line 1, "16" should be changed to -- 17 -- because there is no second XOR gate in claim 16.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 6-7, 11 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,799,048, issued to Farjad-Rad et al.

As per claim 6, Farjad discloses a half-rate phase detector (figure 3) for indicating a phase difference between an incoming data signal (DATA) and a clock signal (CLK1) synthesized from the incoming data signal (using a PLL structure to synthesize), comprising:

a first latch circuit (the combination of latches 32 and 34) for combining a first delayed version of the incoming data signal (the DATA signal can be read as the first delayed version of the incoming data signal when considering a delay time caused by the circuit which receives the incoming data signal and outputs the DATA signal) with alternate transitions of a first delayed version of the clock signal (signal CLK1 has alternate transitions because it is a clock signal, CLK1 is delayed by the VCO circuit 22) to produce first precursor signals (DA1 and DB1);

a multiplexer (MUX 36) connected to the first latch circuit for multiplexing the first precursor signals (MUX 36 receives the first precursor signals DA1 and DB1) in response to a second delayed version of the clock signal (delay circuit 38 causes the second delayed version of the clock signal, column 4, lines 26-27) to produce a multiplexed signal (the signal D1); and

a first logic gate (XOR gate 16) connected to the multiplexer for combining the multiplexed signal (D1) with a second delayed version of the incoming data signal (delay circuit 50 causes the second delayed version of the data signal, column 4, lines 29-30) to produce a phase signal (X1) indicative of a phase difference between the incoming data signal and the clock signal.

As per claim 7, the recited first XOR gate reads on the XOR gate 16.

As per claim 11, Farjad discloses half-rate phase detector (figure 3) for detecting a phase difference between a data signal and a clock signal, comprising:

an input for receiving the data signal (the input of the circuit which receives the transmitted data bits to produce the DATA signal, not shown, column 1, lines 12-13);

a first latch (latch 32) for sampling a first delayed version of the data signal (DATA, the delay is caused by the circuit which receives the transmitted data bits) in response to a first delayed version of the clock signal (CLK1, the delay is caused by the VCO 22), the first latch having an output (output Q of latch 32, the signal DA1);

a second latch (latch 34) for sampling the first delayed version of the data signal in response to the inverse of the first delayed version of the clock signal (/CLK1), the second latch having an output (output Q of latch 34, the signal DB1);

a multiplexer (MUX 36) having a first input connected to the output of the first latch (DA1), a second input connected to the output of the second latch (DB1), a control input for receiving a second delayed version of the clock signal (the delay circuit 38 generates the second delayed version of the clock signal), and an output (D1); and

a first exclusive-OR gate (XOR 16) having a first input connected to the output of the multiplexer (D1), a second input for receiving a second delayed version of the data signal (the delay circuit 50 generates the second delayed version of the date signal), and an output for producing a phase signal (X1) representing a phase difference between the data signal and the clock signal.

As per claim 1, this claim is merely a method to operate the phase detector having the structure discussed in claim 6. Since Farjad teaches the structure, the method to operate is inherently taught.

As per claim 2, this claim is rejected for the same reason noted in claim 7.

As per claim 16, this claim is merely a method to operate the phase detector having the structure discussed in claim 11. Since Farjad teaches the structure, the method to operate is inherently taught.

***Allowable Subject Matter***

4. Claims 3-5, 8-10, 12-15 and 17-20 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 8-10 are allowable because the prior art of record fails to disclose or suggest the inclusion of a second logic gate for combining the second precursor signals to produce a reference signal as recited in claim 8. The recited limitation defines patentability over the prior art of record because it defines a distinguished structure of the phase detector which is not taught by the art of record, alone or in combination.

Claims 3-5, 12-15 and 17-20 are allowable for the same reason noted in claim 8.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Minh Nguyen whose telephone number is **571-272-1748**. The examiner can normally be reached on Monday, Tuesday, Thursday, Friday 7:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

6/17/05

Minh Nguyen
Primary Examiner
Art Unit 2816